WHAT IS CLAIMED IS:

1. A semiconductor device having an insulating film, comprising:

an interconnect groove or a via hole which is formed in the insulating film;

an interconnect pattern or a via hole which is buried in the interconnect groove or the via hole; and

a substantially flat hard mask which is formed on the interconnect pattern and which is provided with an opening portion having a width narrower than a space between adjacent interconnect patterns and which is made of a material that is etched selectively with the insulating film.

2. A semiconductor device claimed in claim 1, wherein:

the hard mask comprises a slit-like opening portion which is formed in an extending direction of the interconnect pattern located below the hard mask.

3. A semiconductor device having an insulating film, comprising:

an interconnect groove or a via hole which is formed in the insulating film;

an interconnect pattern or a via hole which is buried in the interconnect groove or the via hole;

a first layer interconnect pattern;

a second layer interconnect pattern which is formed on the first layer interconnect pattern;

a third layer interconnect pattern which is formed on the second layer interconnect pattern, the third layer interconnect pattern being connected to the first layer interconnect pattern through a third-first layer interconnection via penetrating a space between adjacent second layer interconnect patterns; and

a substantially flat hard mask which is formed on the second interconnect pattern and which is provided with an opening portion specifying a shape of the third-first layer interconnection via and which is made of a material

that is etched selectively with the insulating film.

4. A semiconductor device claimed in claim 3, wherein:

the hard mask comprises a slit-like opening portion which is formed in an extending direction of the interconnect pattern located below the hard mask.

5. A method of manufacturing a semiconductor device, comprising the steps of:

forming an interconnect groove or a via hole in a insulating film formed on a substrate;

forming an interconnect pattern or a via by burying an interconnect material containing at least one of copper and tungsten in the interconnect groove or the via hole; and

forming a substantially flat hard mask which is made of a material that is etched selectively with the insulating film except for a region having a width narrower than a space between adjacent interconnect patterns on the interconnect pattern after forming the interconnect pattern.

6. A method as claimed in claim 5, wherein:

the opening portion of the hard mask is formed to a slit form in an extending direction of the interconnect pattern located below the hard mask.

7. A method of manufacturing a semiconductor device, comprising the steps of:

forming an interconnect groove or a via hole in a insulating film formed on a substrate;

forming an interconnect pattern or a via by burying an interconnect material containing at least one of copper and tungsten in the interconnect groove or the via hole;

forming a first cover insulating film on the interconnect pattern after forming the interconnect pattern;

forming a first resist pattern including an opening portion having a width narrower than a space between adjacent interconnect patterns on the first

cover insulating film;

etching the first cover insulating film by using the first resist pattern as a first mask;

depositing a second cover insulating film which is etched selectively with the first cover insulating film so as to cover the first cover insulating film after removing the first resist pattern;

forming a substantially flat hard mask which is buried with the first cover insulating film between the second cover insulating film by polishing the second cover insulating film by etchback or CMP;

forming an interlayer insulating film on the hard mask;

forming a second resist pattern having an opening portion which is equivalent to or wider than that of the first cover insulating film on the interlayer insulating film; and

forming the via hole by etching the interlayer insulating film and the first cover insulating film using the second resist pattern as a second mask and by etching the insulating film using the second cover insulating film as a third mask.

8. A method as claimed in claim 7, wherein:

the second cover insulating film is formed by a material that is etched selectively with the insulating film and the interlayer insulating film.

9. A method as claimed in claim 7, wherein:

the opening portion of the hard mask is formed to a slit form in an extending direction of the interconnect pattern located below the hard mask.

10. A method of manufacturing a semiconductor device, comprising the steps of:

forming an interconnect groove or a via hole in a insulating film formed on a substrate;

forming an interconnect pattern or a via by burying an interconnect material containing at least one of copper and tungsten in the interconnect

groove or the via hole;

forming a cover insulating film on the interconnect pattern after forming the interconnect pattern;

forming a first resist pattern including an opening portion having a width narrower than a space between adjacent interconnect patterns on the cover insulating film;

forming a substantially flat hard mask by etching the cover insulating film using the first resist pattern as a first mask;

forming an interlayer insulating film on the hard mask after removing the first resist pattern;

forming a second resist pattern having an opening portion which is equivalent to or wider than that of the first cover insulating film on the interlayer insulating film; and

forming the via hole by etching the interlayer insulating film using the second resist pattern as a second mask and by etching the insulating film using the second cover insulating film as a third mask.

11. A method as claimed in claim 10, wherein:

the cover insulating film is formed by a material that is etched selectively with the insulating film and the interlayer insulating film.

12. A method as claimed in claim 10, wherein:

the opening portion of the hard mask is formed to a slit form in an extending direction of the interconnect pattern located below the hard mask.